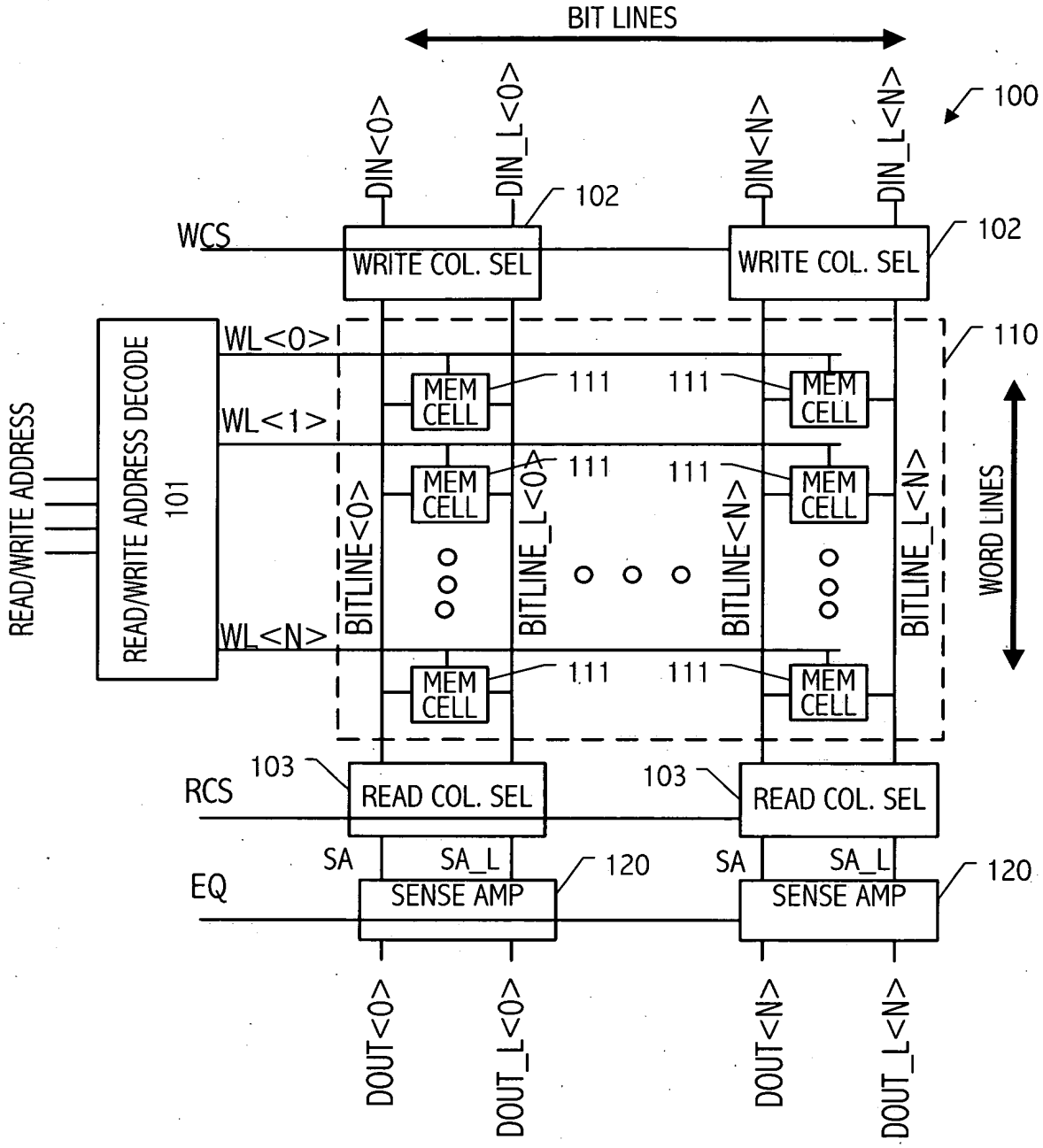
BIT LINES
100
DIN<0>
DIN_L<0>
DIN<N>
DIN_L<N>
102
WCS
WRITE COL. SEL
WRITE COL. SEL
READ/WRITE ADDRESS
READ/WRITE ADDRESS DECODE
101
WL<0>
WL<1>
WL<N>
MEM CELL
111
110
BITLINE<0>
BITLINE_L<0>
BITLINE<N>
BITLINE_L<N>
WORD LINES
103
RCS
READ COL. SEL
READ COL. SEL
SA
SA_L
EQ
SENSE AMP
120
DOUT<0>
DOUT_L<0>
DOUT<N>
DOUT_L<N>

FIG. 1

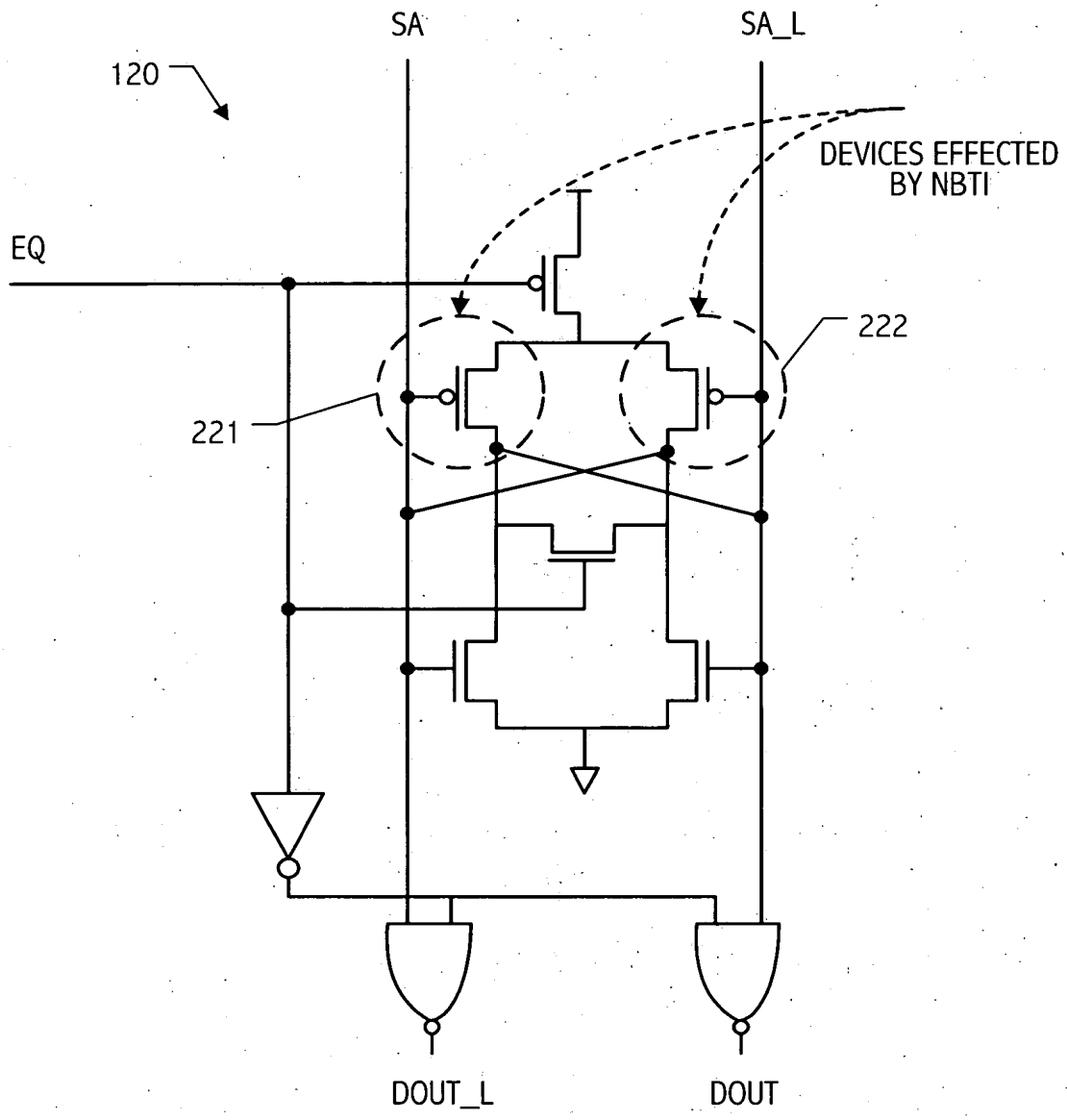


FIG. 2

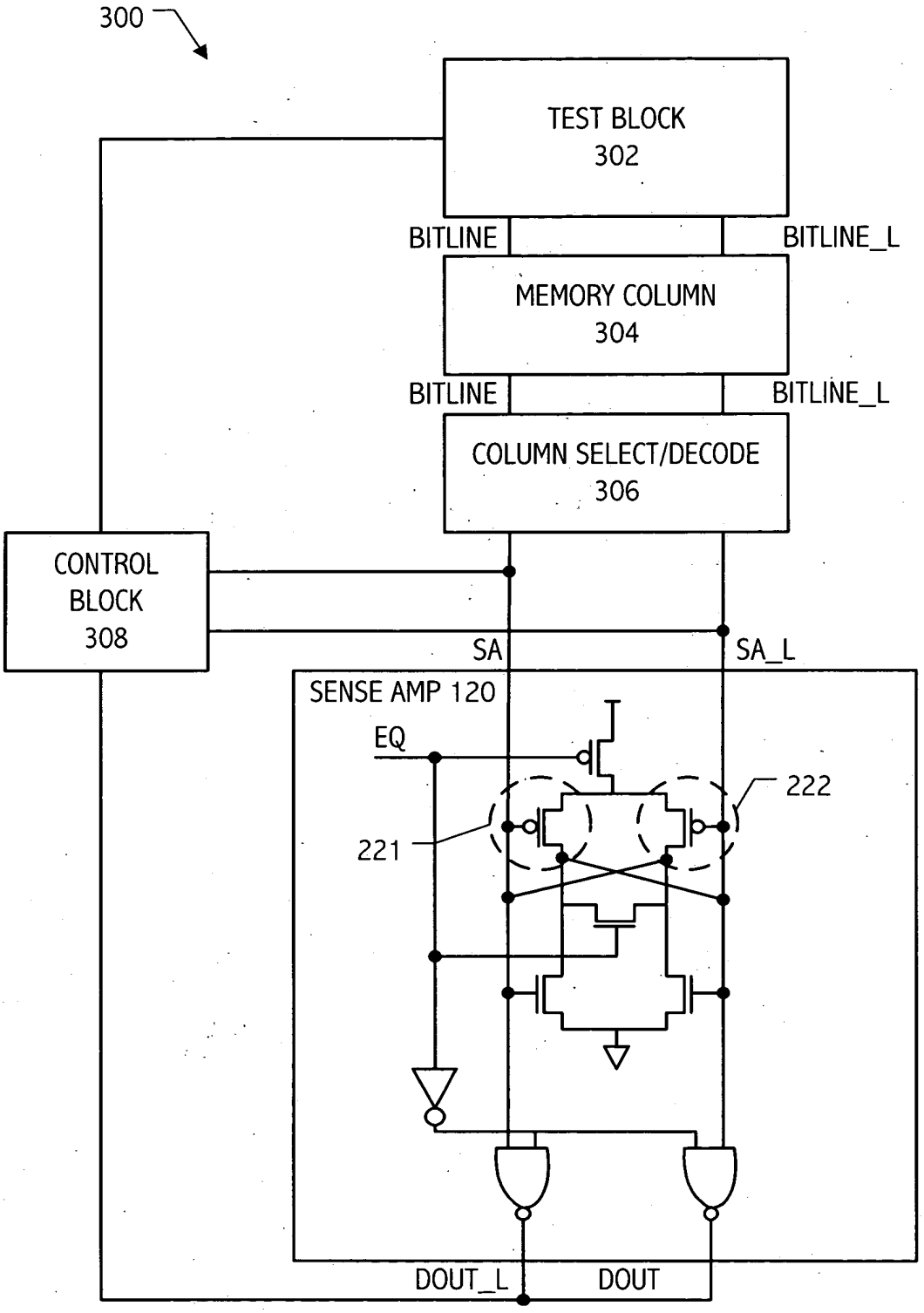
300
TEST BLOCK
302
BITLINE
BITLINE_L
MEMORY COLUMN
304
BITLINE
BITLINE_L
COLUMN SELECT/DECODE
306
CONTROL
BLOCK
308
SA
SA_L
SENSE AMP 120
EQ
222
221
DOUT_L
DOUT

FIG. 3

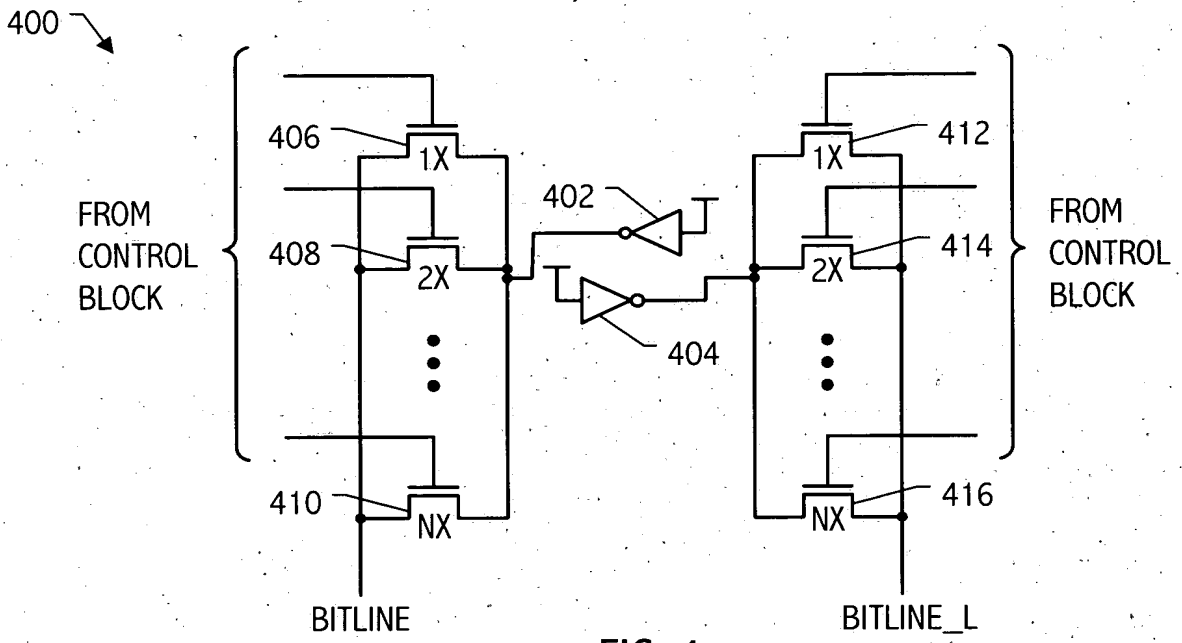
400
406
1X
408
2X
410
NX
FROM CONTROL BLOCK
402
404
412
1X
414
2X
416
NX
FROM CONTROL BLOCK
BITLINE
BITLINE_L

FIG. 4

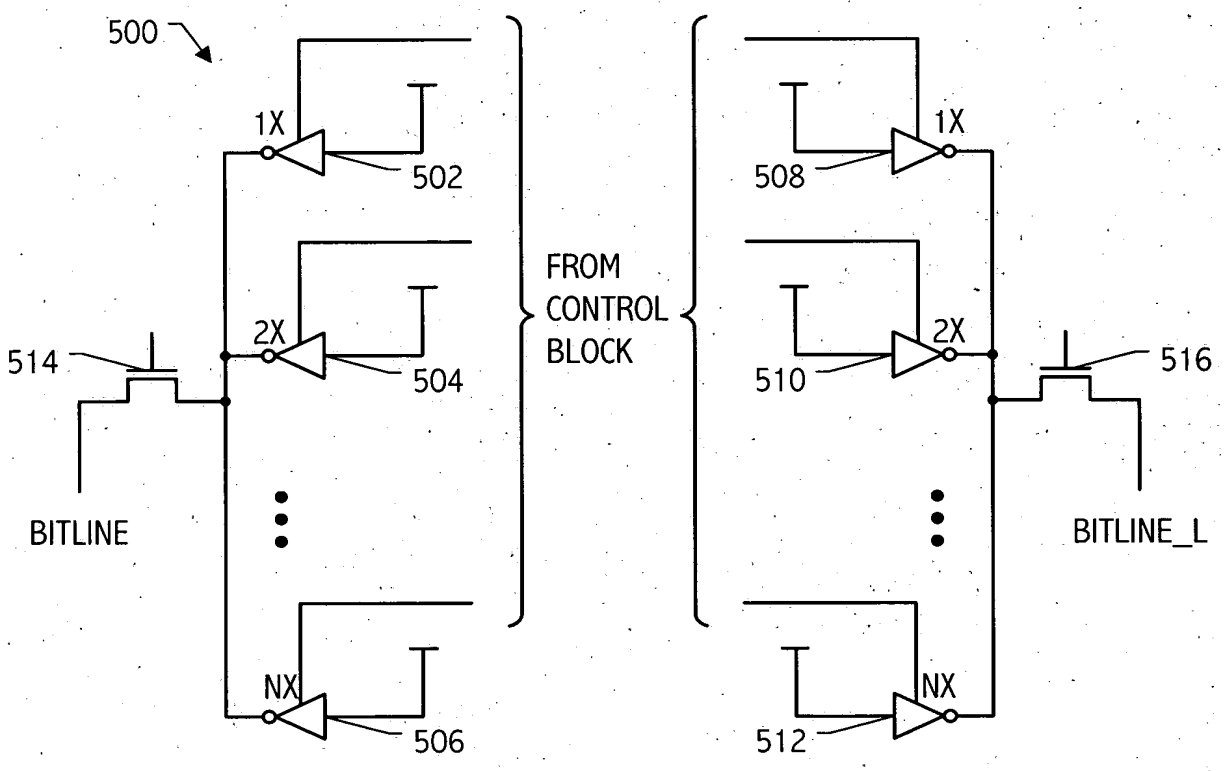
500
1X
502
2X
504
NX
506
514
BITLINE
FROM CONTROL BLOCK
508
1X
510
2X
512
NX
516
BITLINE_L

FIG. 5

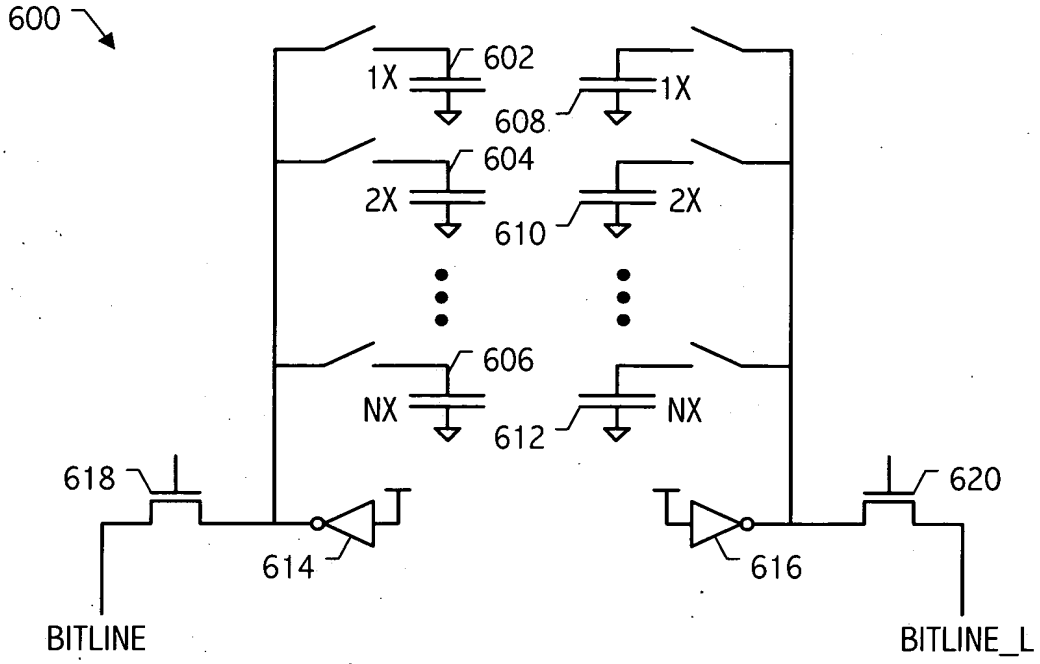
600
602
1X
608
1X
604
2X
610
2X
606
NX
612
NX
618
620
614
616
BITLINE
BITLINE_L

FIG. 6

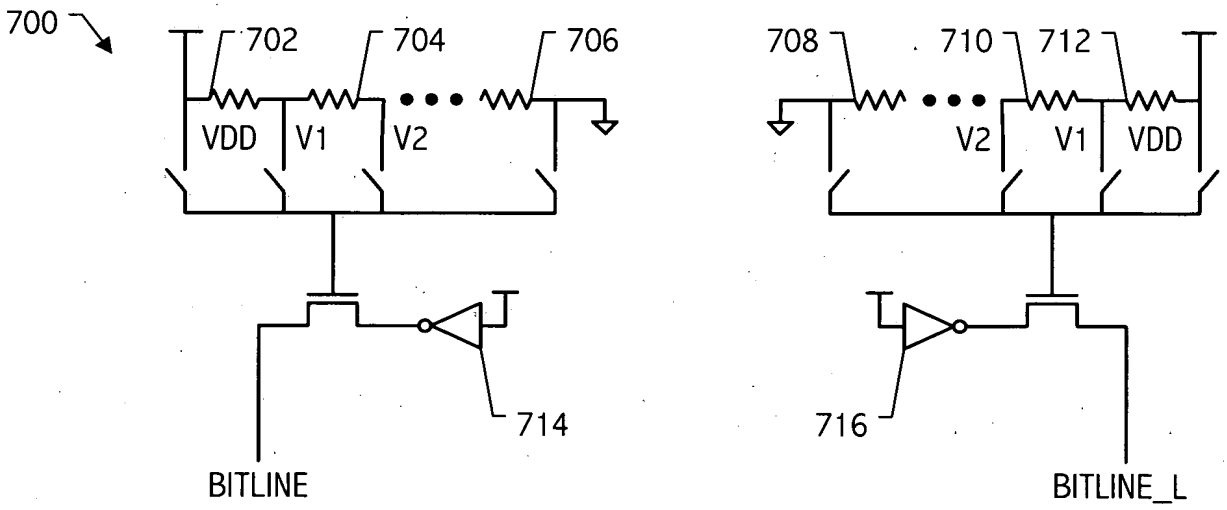
700
702
704
706
VDD
V1
V2
708
710
712
V2
V1
VDD
714
716
BITLINE
BITLINE_L

FIG. 7